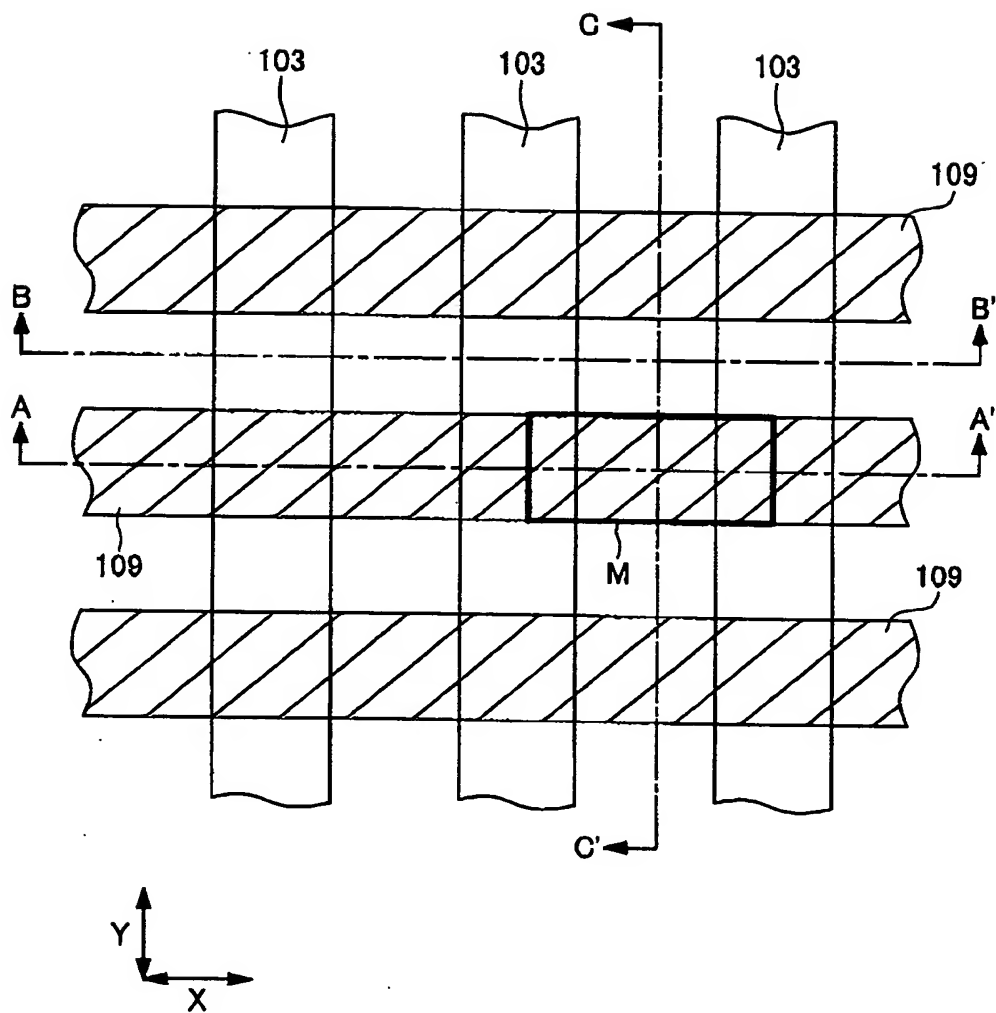
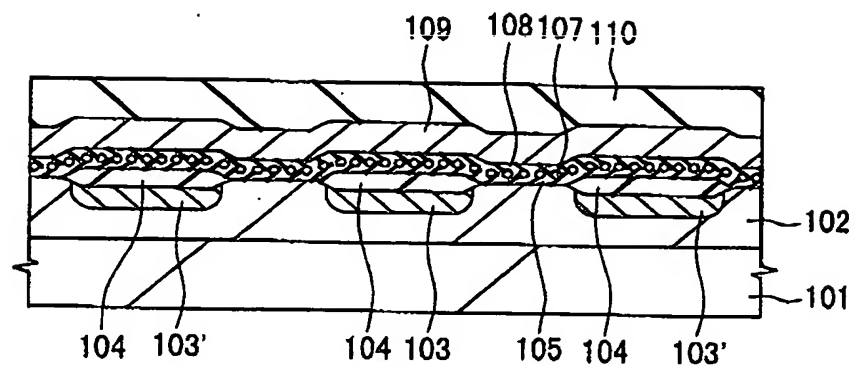


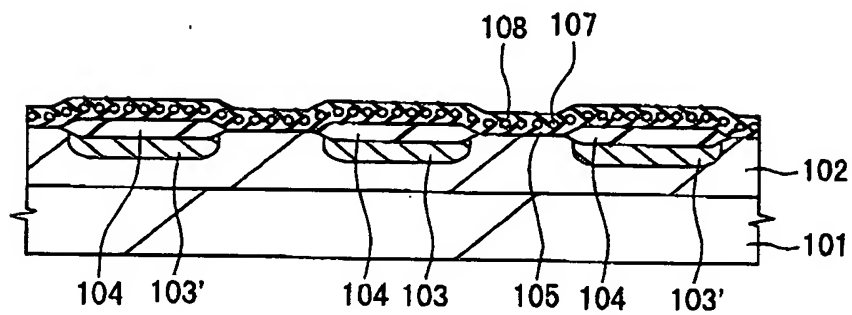
FIG.1



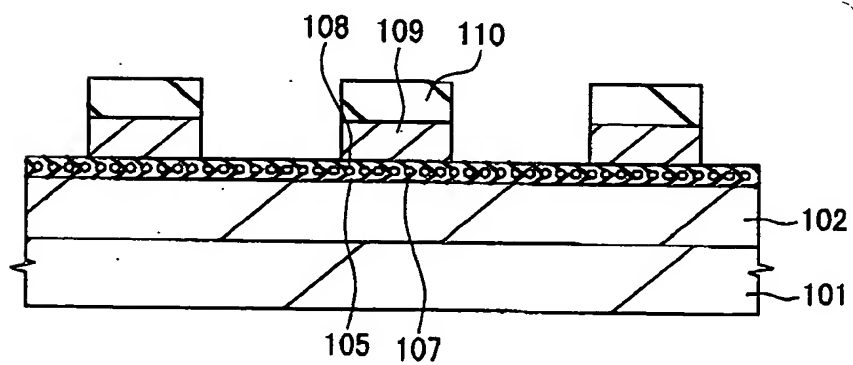
# FIG.2



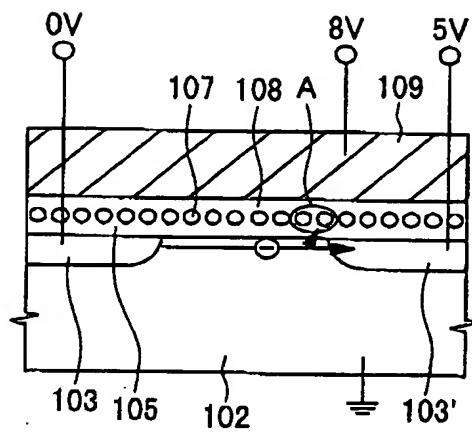
# FIG.3



# FIG.4

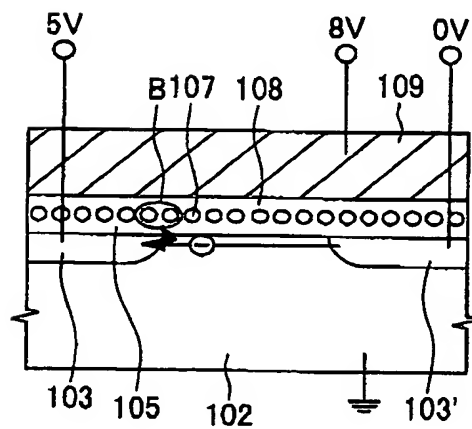


# FIG.5



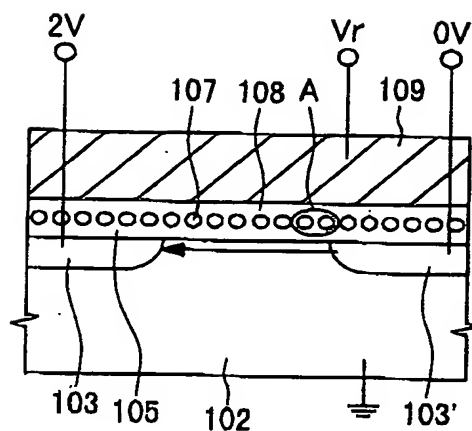
## PROGRAM 1

# FIG.6



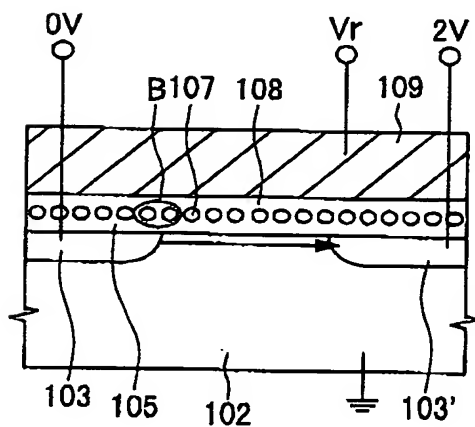
## PROGRAM 2

# FIG.7



READ 1

# FIG.8



READ 2

FIG.9

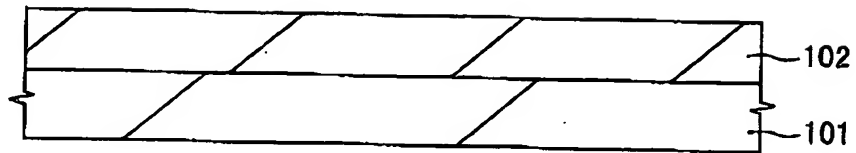


FIG.10

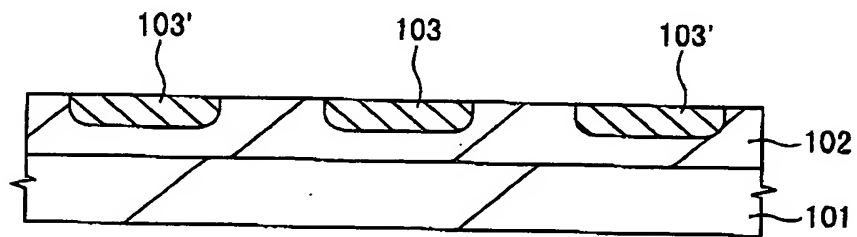


FIG.11

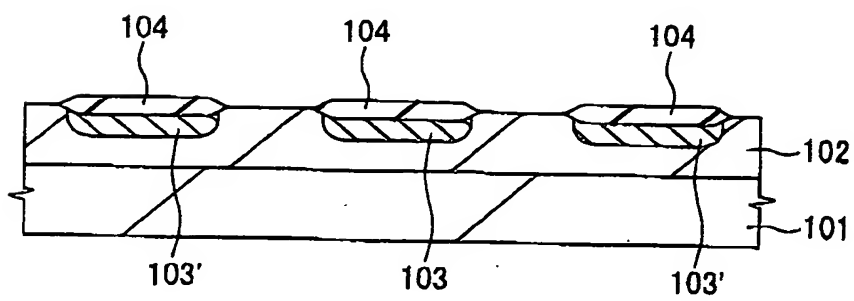


FIG.12

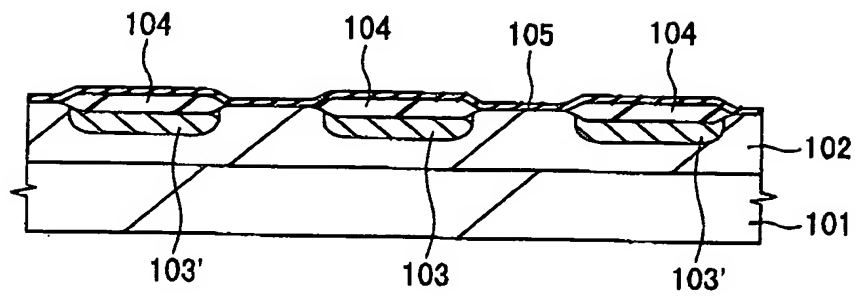


FIG.13

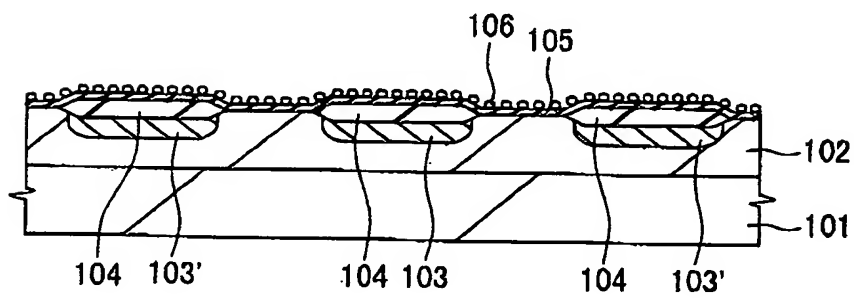


FIG.14

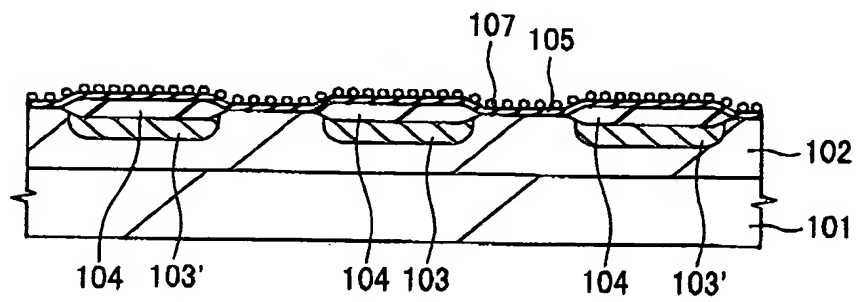


FIG.15

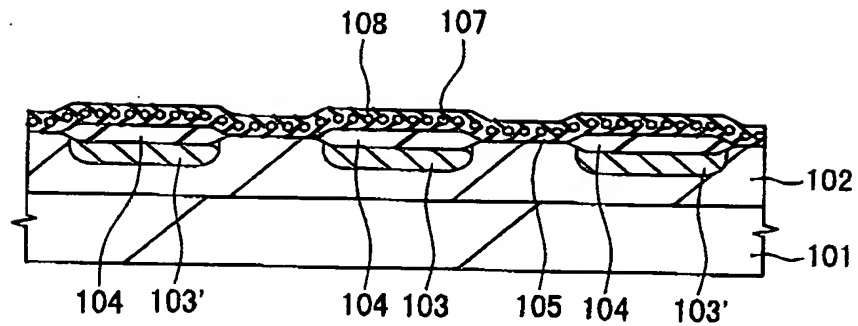


FIG.16

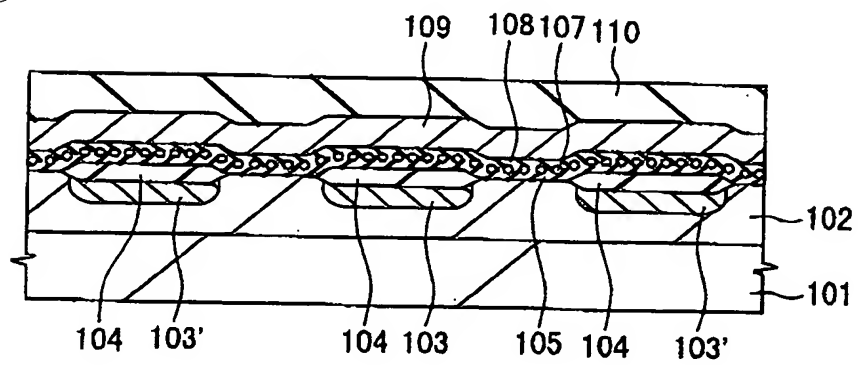


FIG.17

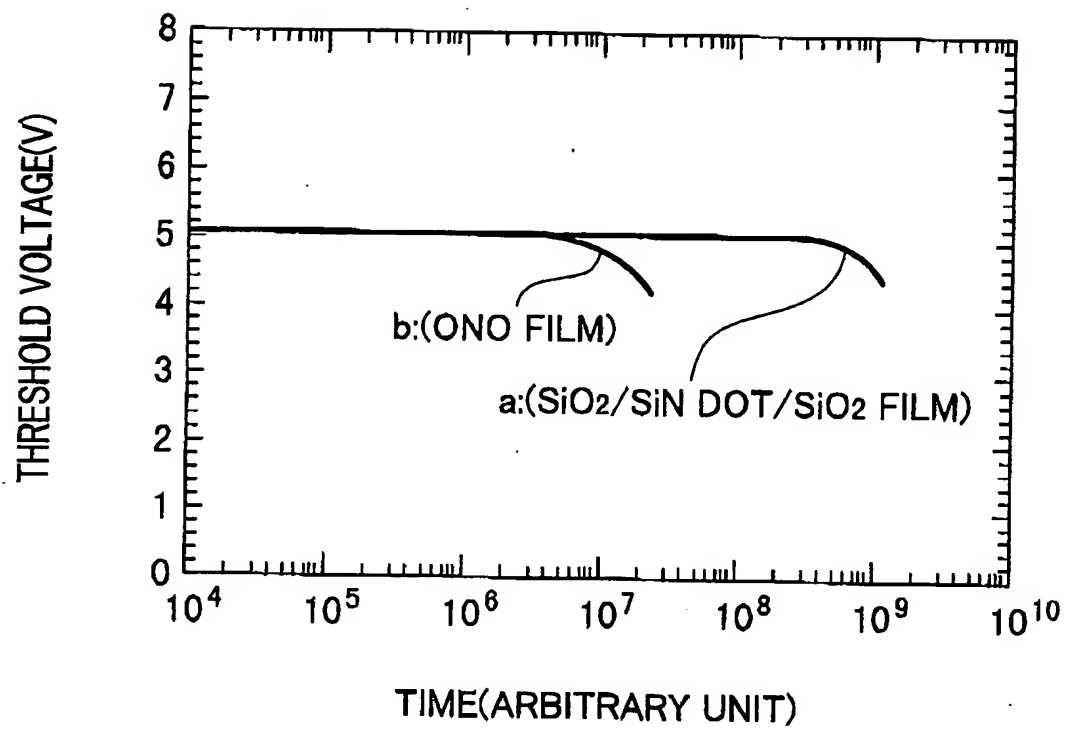




FIG.18

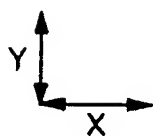
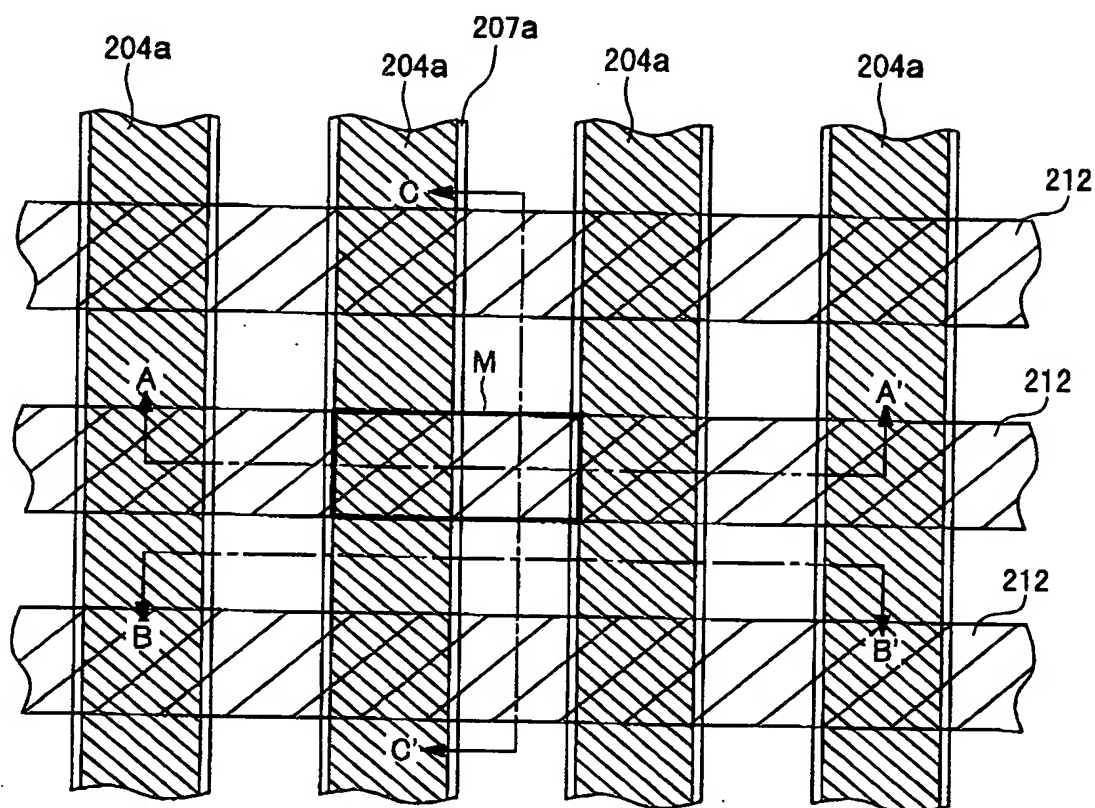
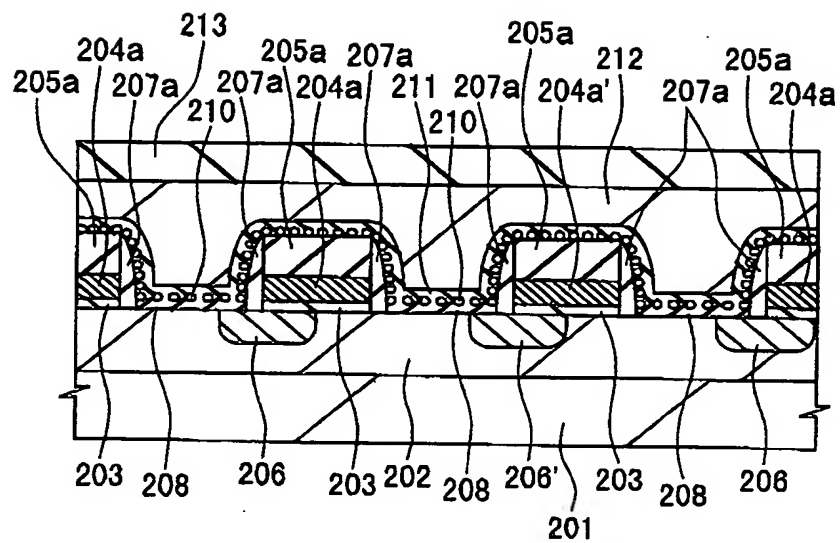
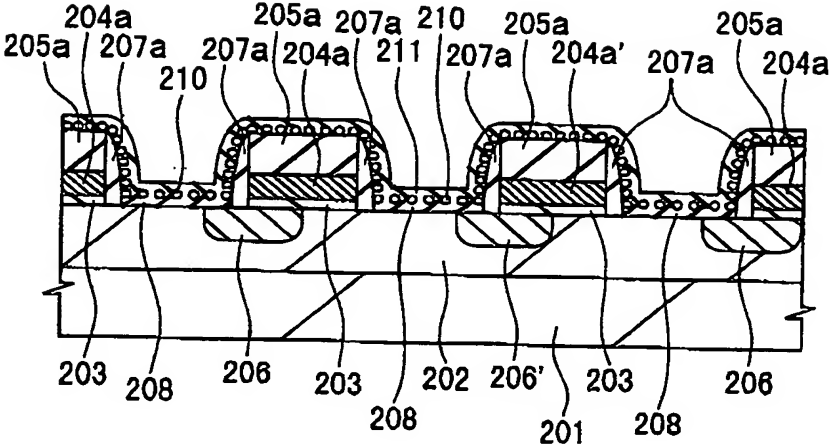


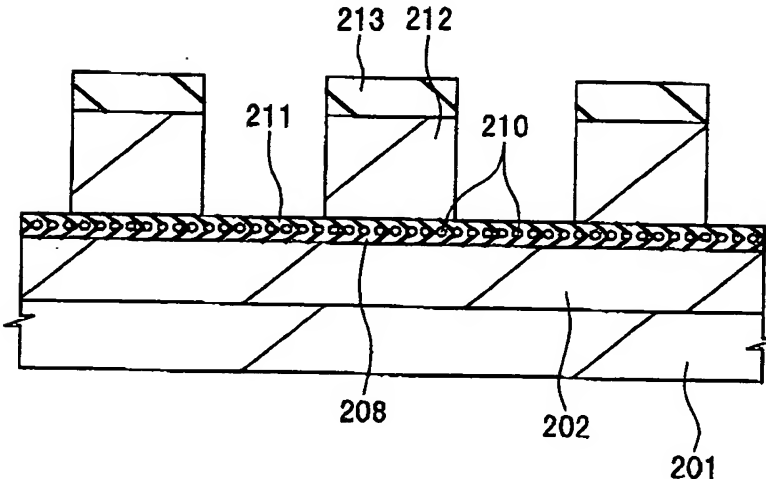
FIG.19



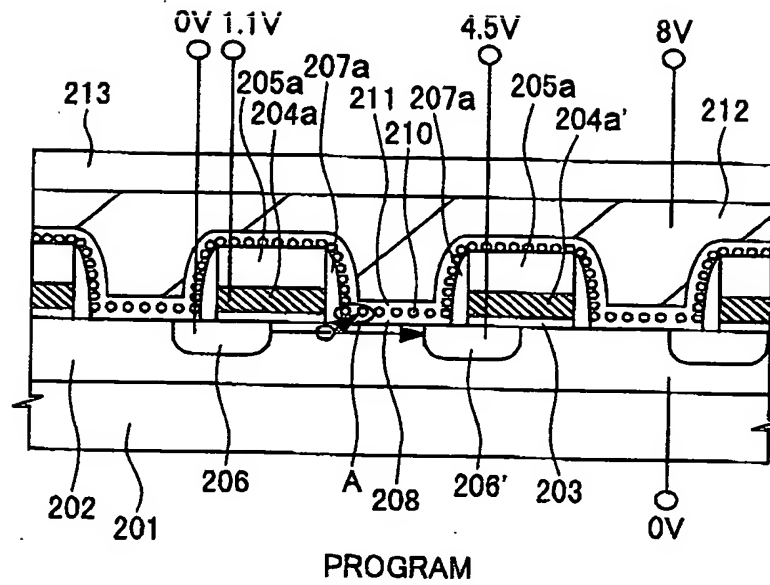
**FIG. 20**



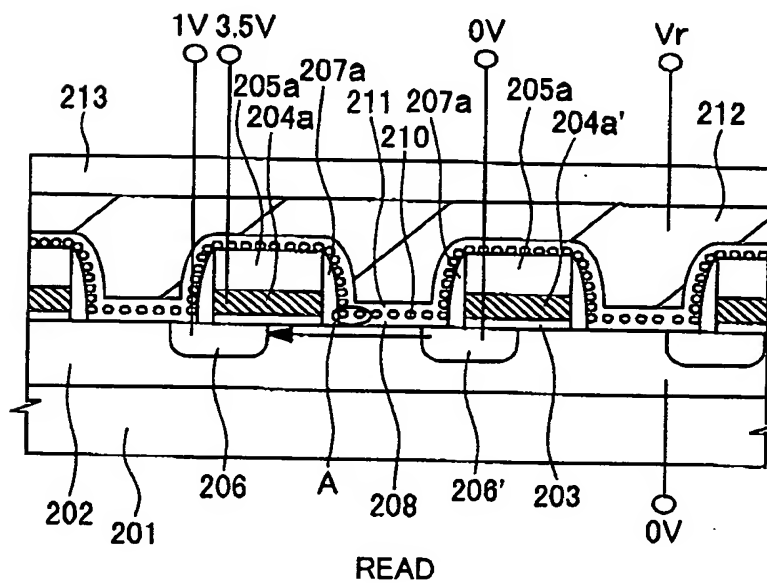
**FIG.21**



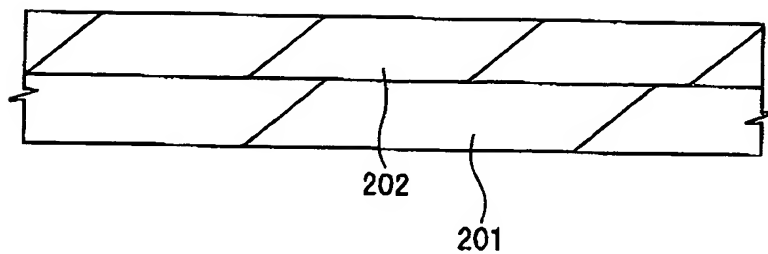
# FIG.22



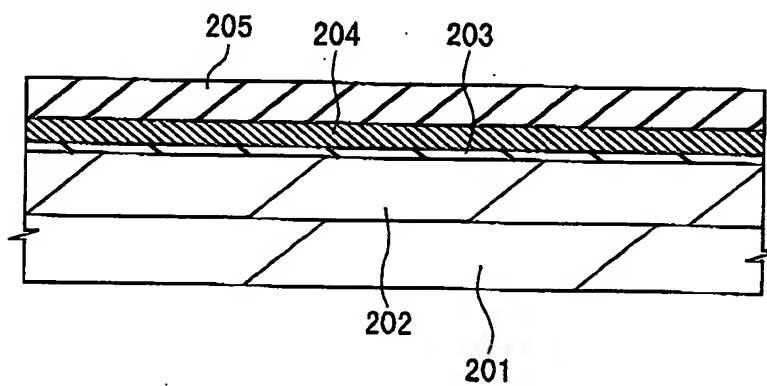
# FIG.23



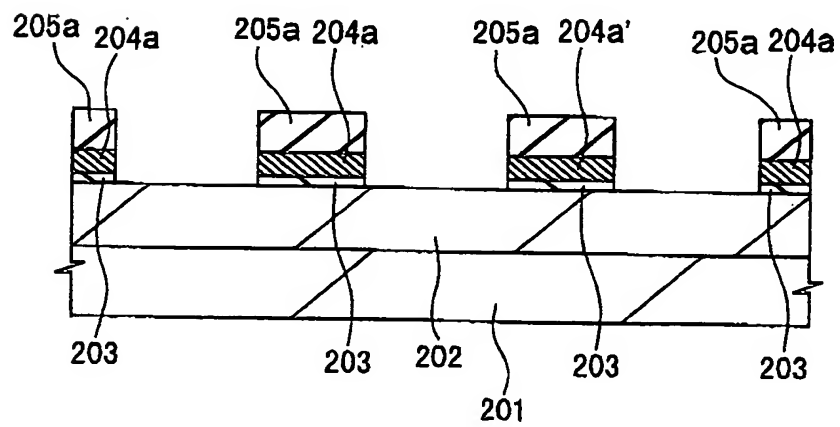
# FIG.24



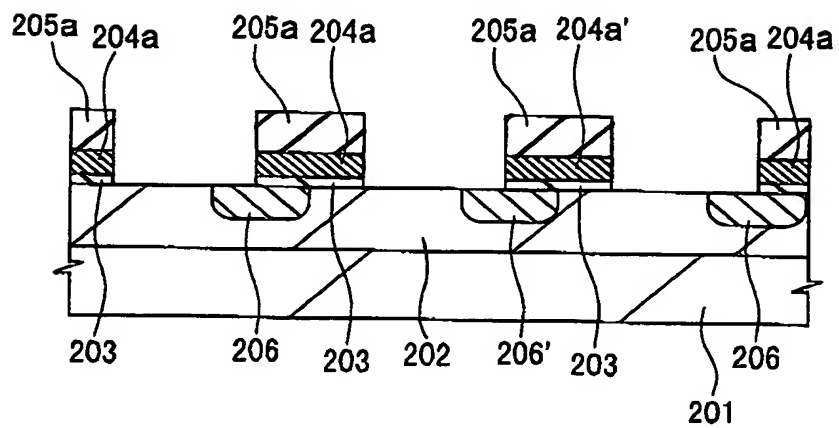
# FIG.25



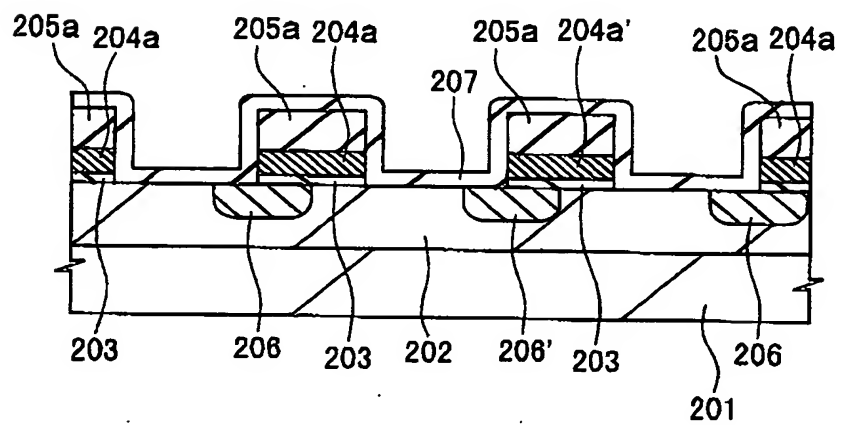
# FIG.26



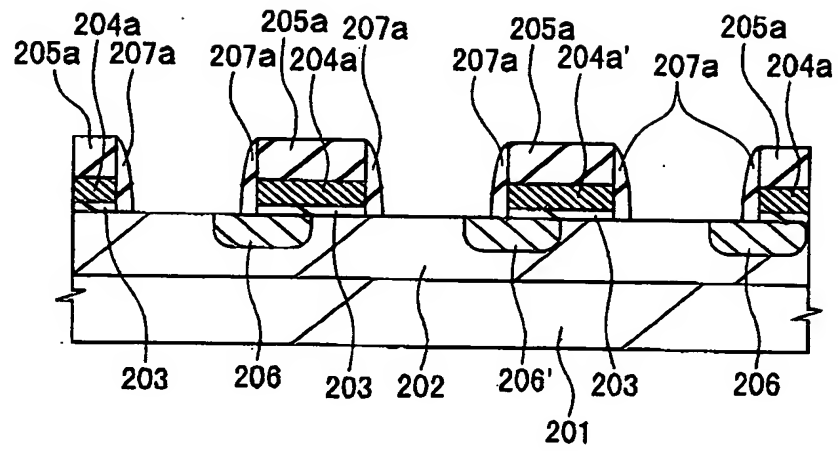
# FIG.27



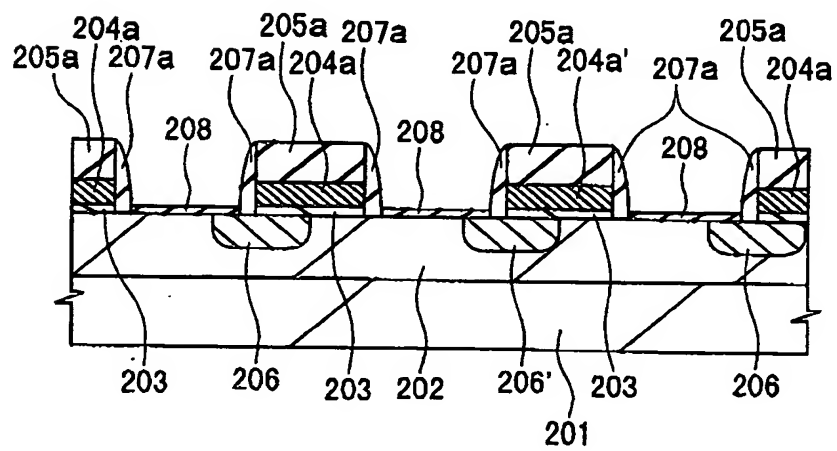
# FIG.28



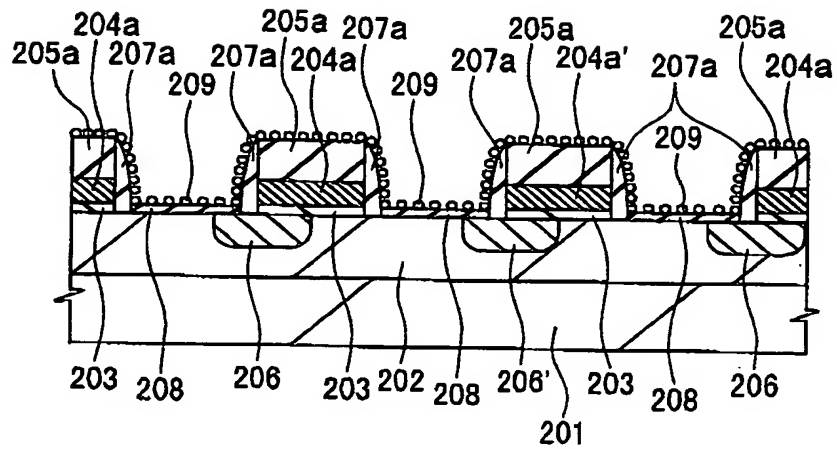
# FIG.29



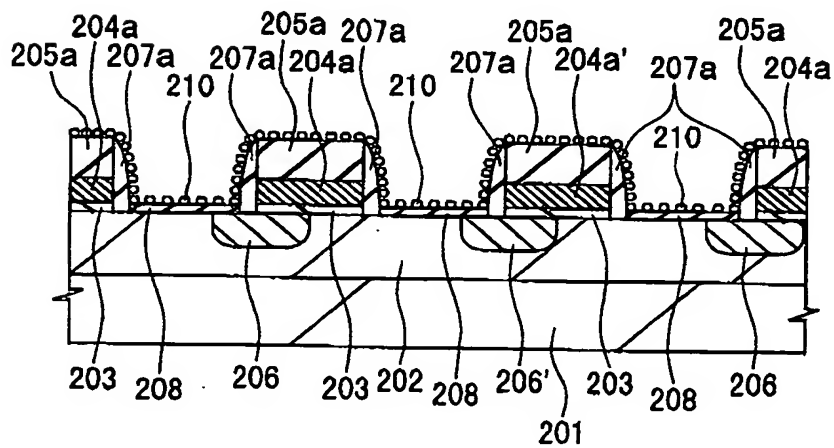
# FIG.30



# FIG.31

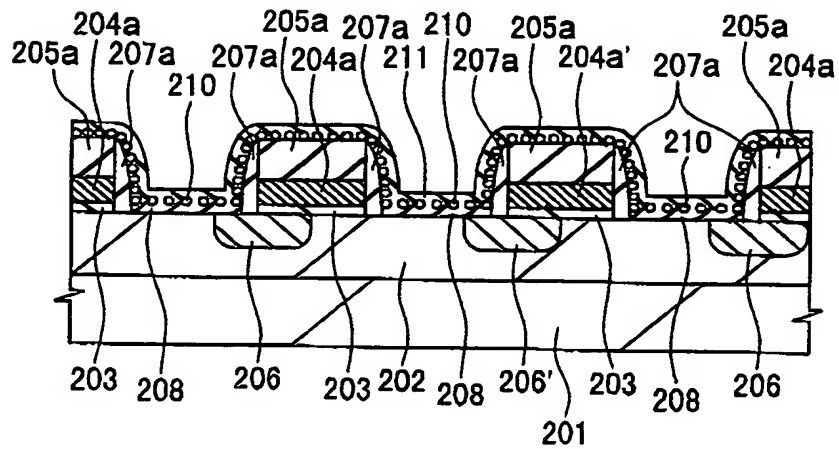


# FIG.32





# FIG.33



# FIG.34

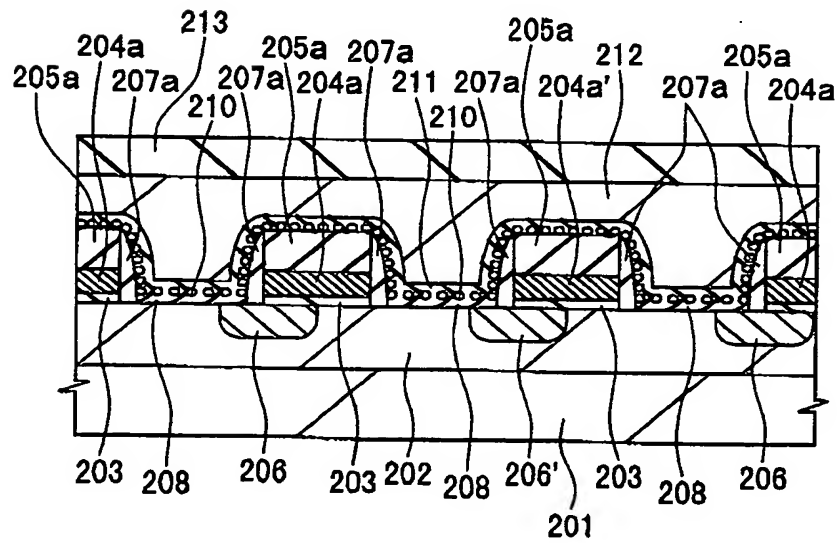
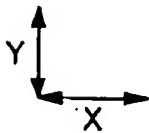
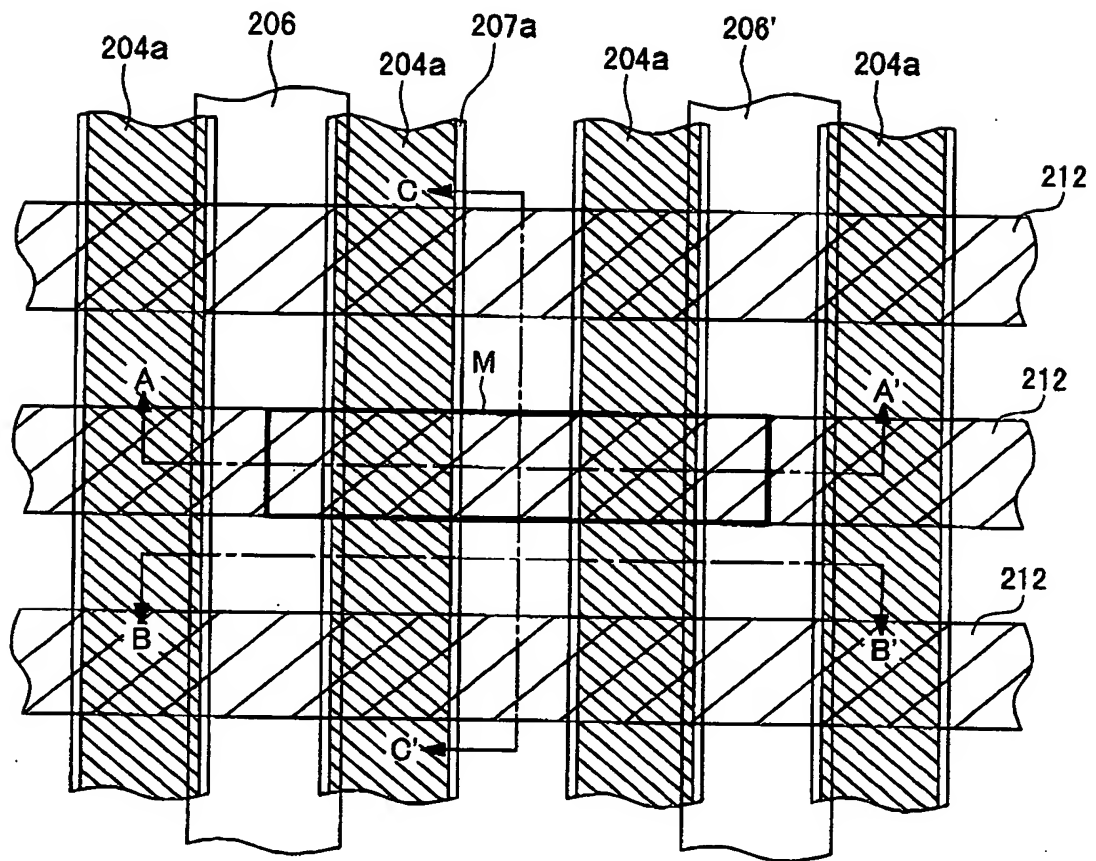
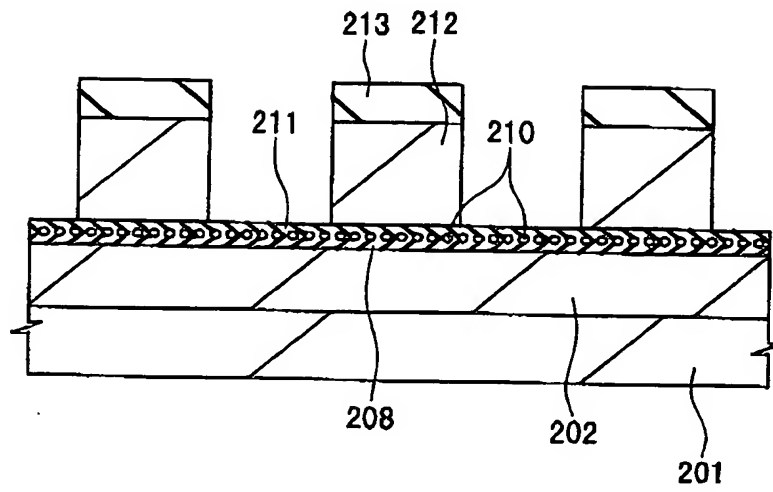


FIG.35

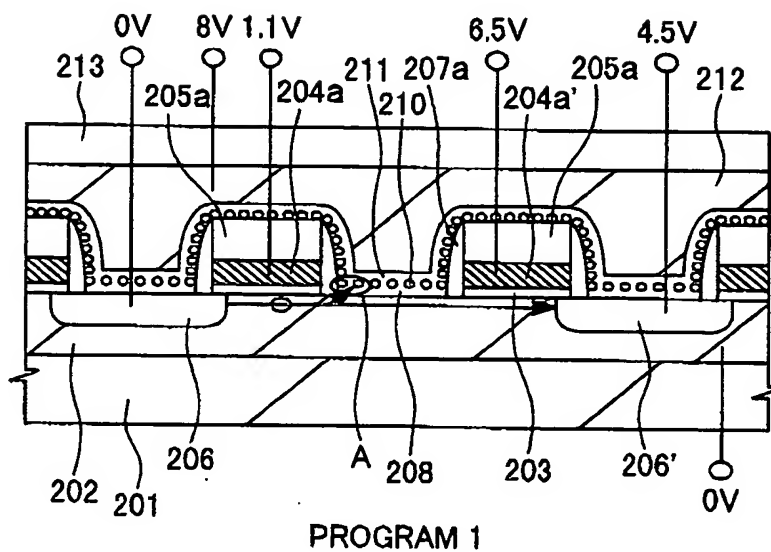


This cross-sectional view shows a semiconductor device with a substrate 201 and a base layer 202. A series of gate structures are formed on the surface, each consisting of a gate stack 203 and a gate cap 206. The gate stacks are separated by spacers 208. The gate caps are formed on top of the gate stacks and are connected to a common layer 204a. The gate stacks are also connected to a common layer 205a. The gate stacks are labeled 204a, 205a, 207a, 210, 205a, 207a, 204a', 207a, 204a. The gate stacks are also labeled 203, 208, 206, 203, 208, 203, 208, 206'.

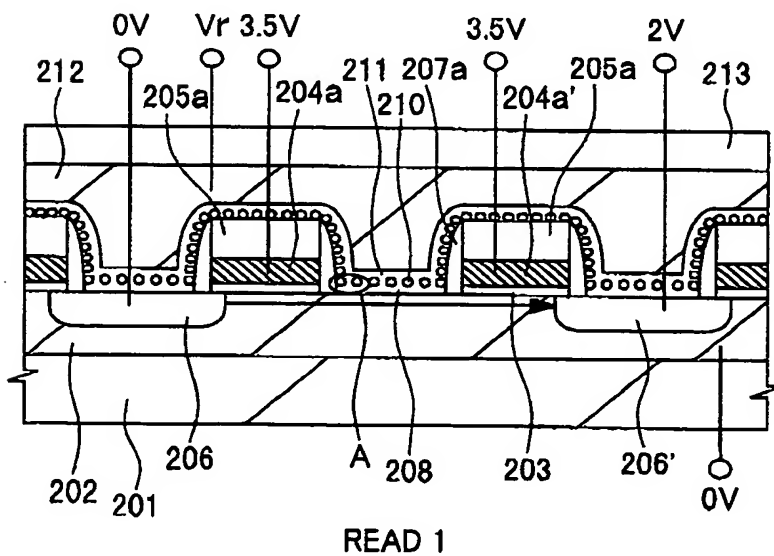
FIG.38



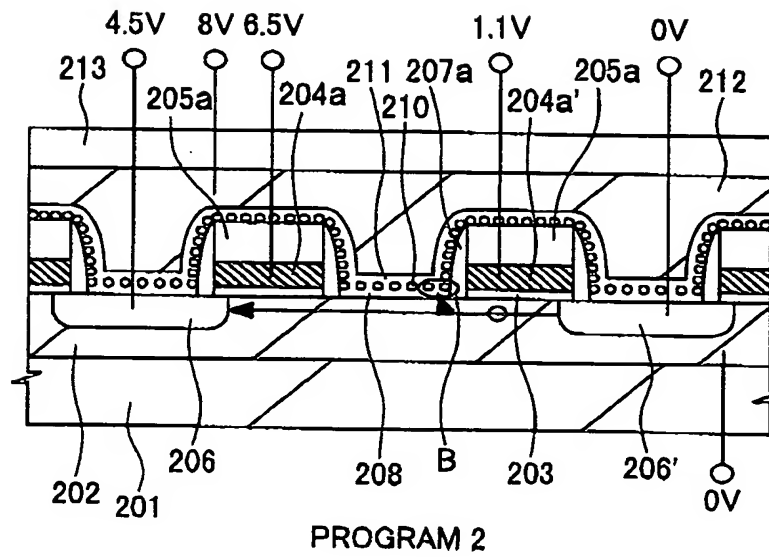
# FIG.39



# FIG.40



# FIG.41



# FIG.42

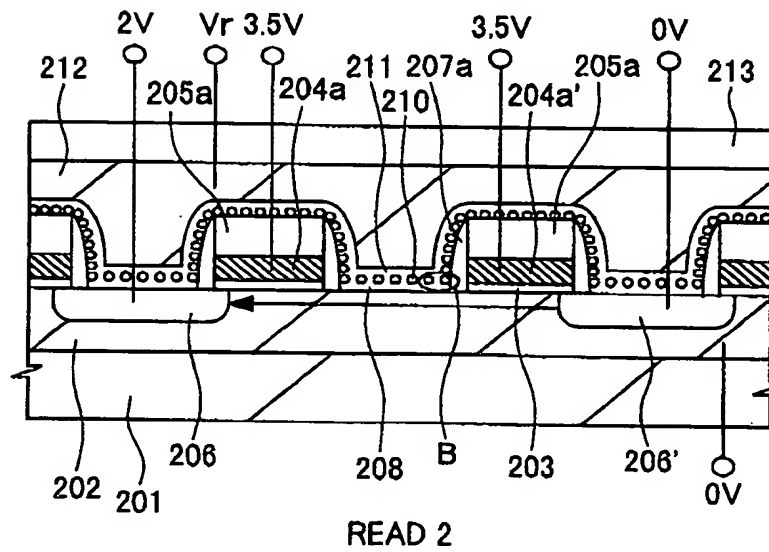


FIG.43

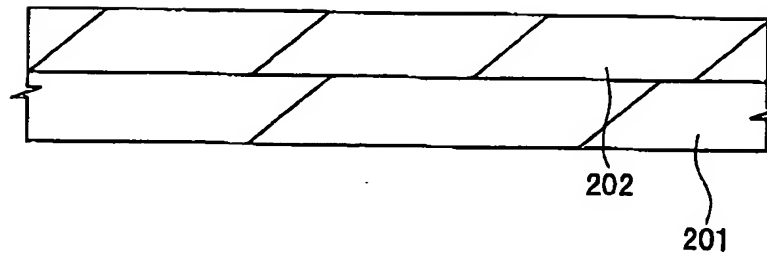


FIG.44

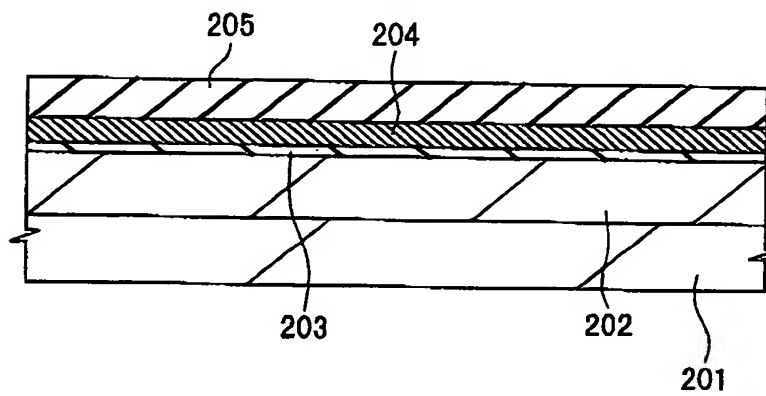
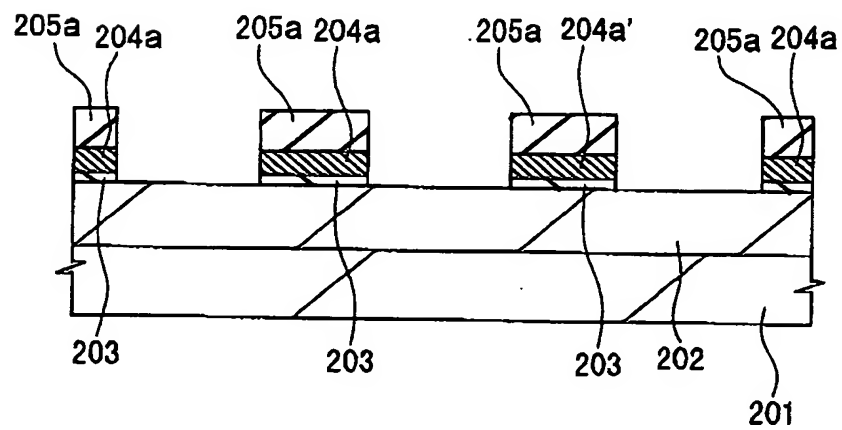
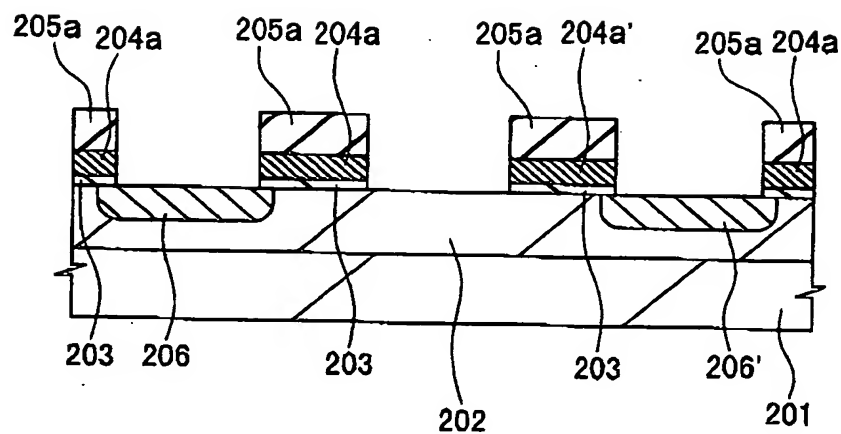


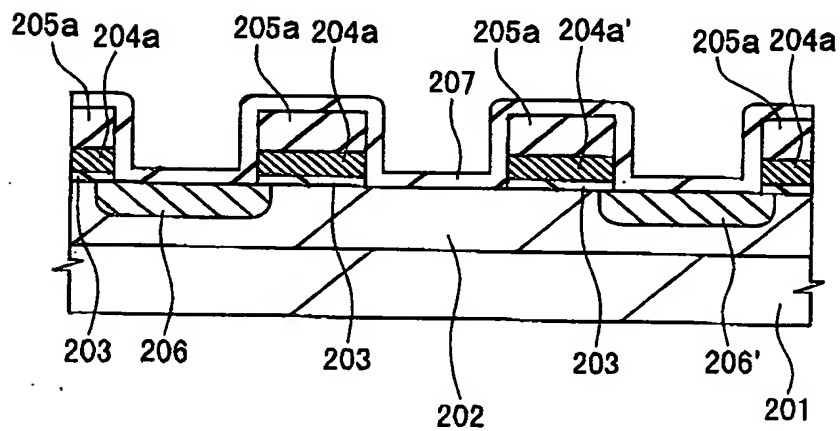
FIG.45



# FIG.46

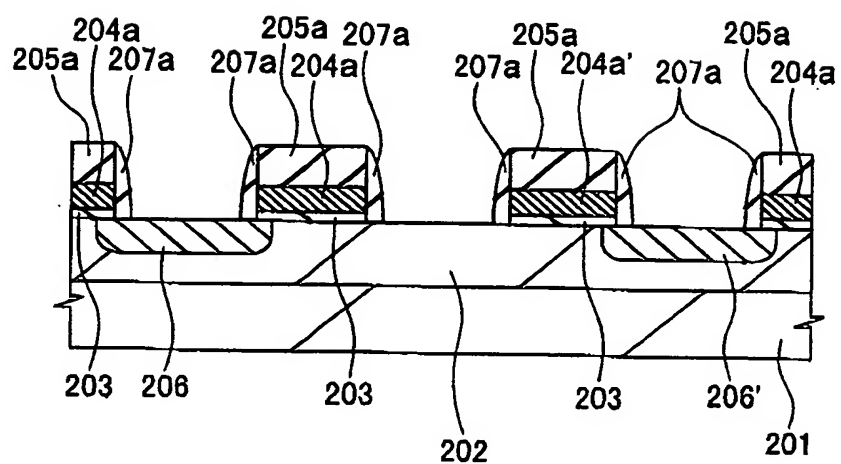


# FIG.47

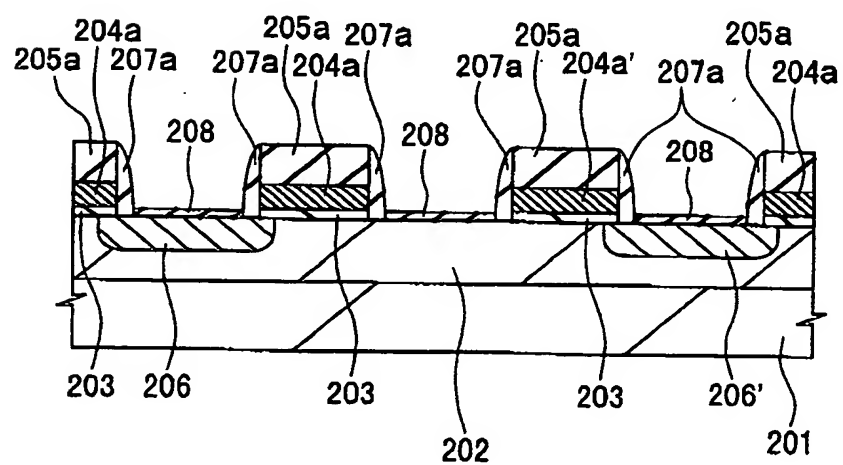




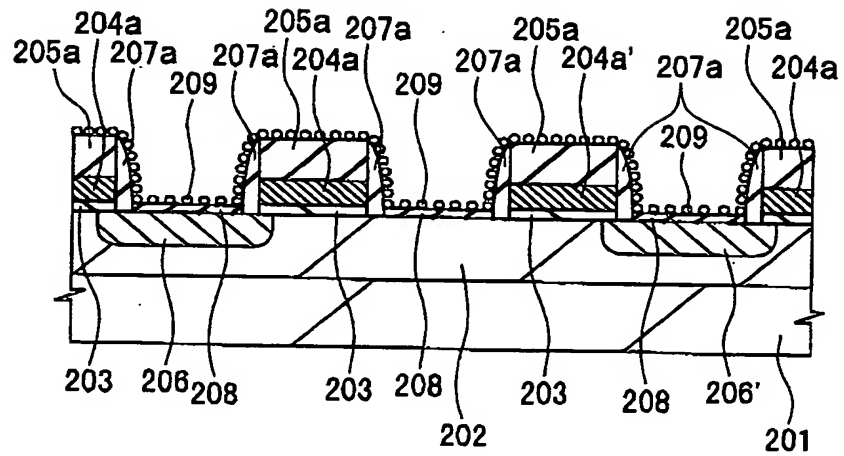
# FIG.48



# FIG.49



# FIG.50



# FIG.51

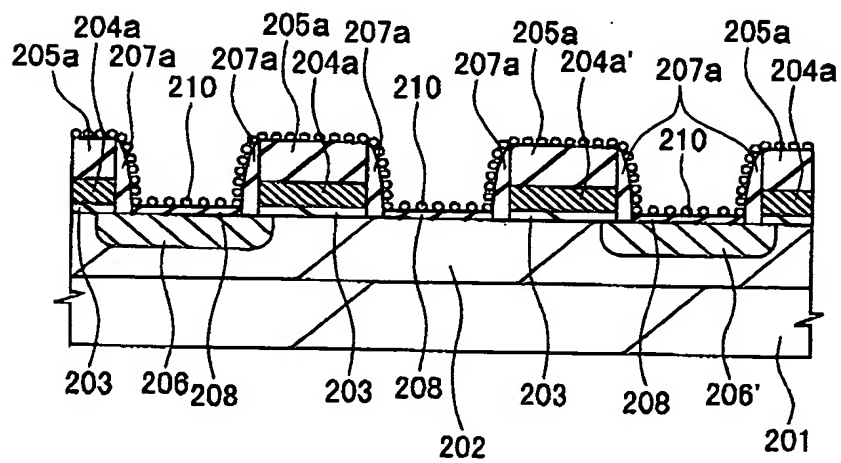


FIG.52

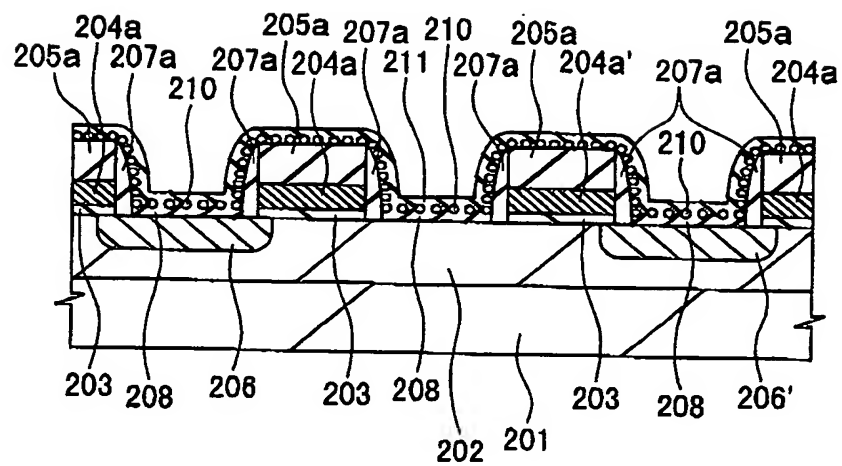


FIG.53

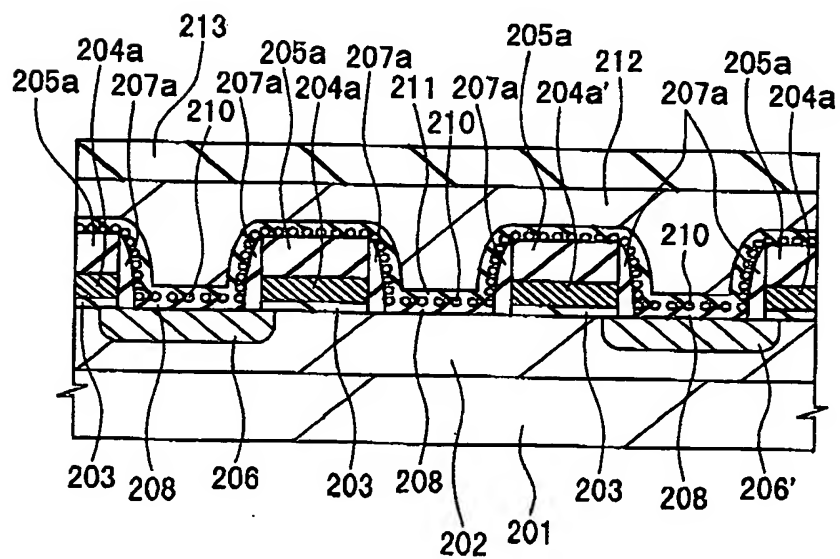


FIG.54

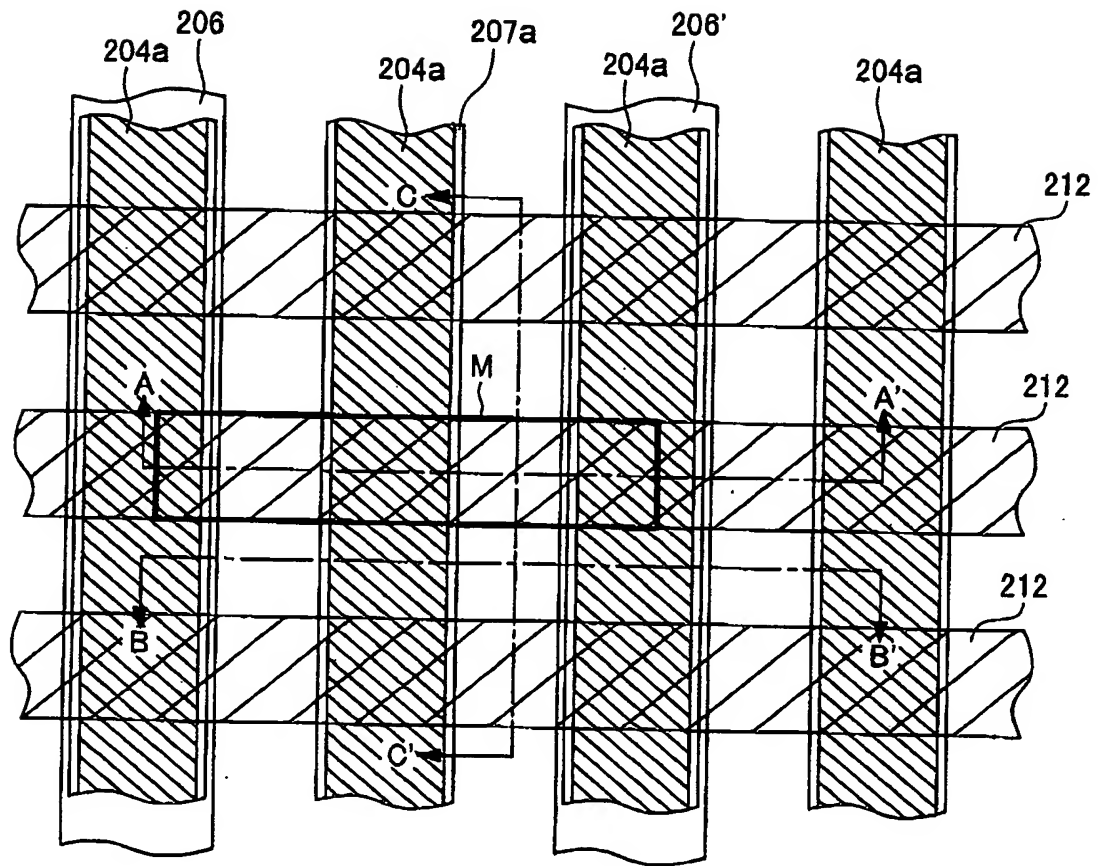
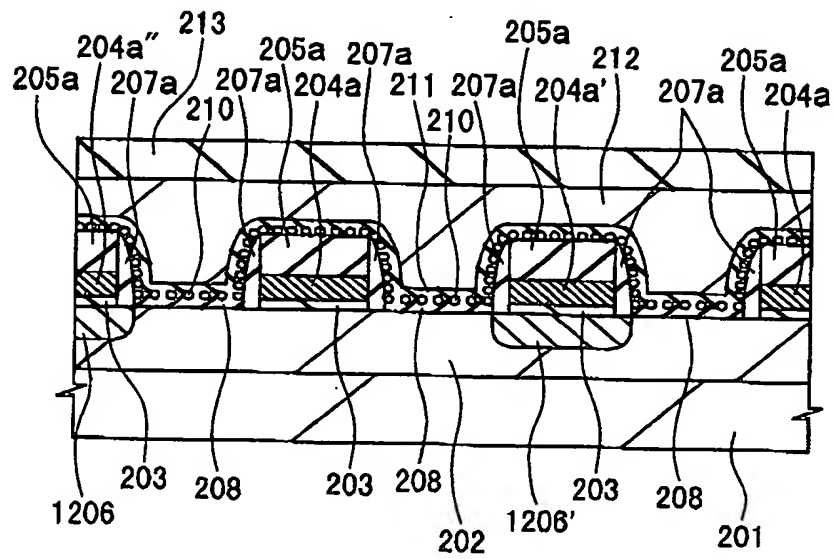
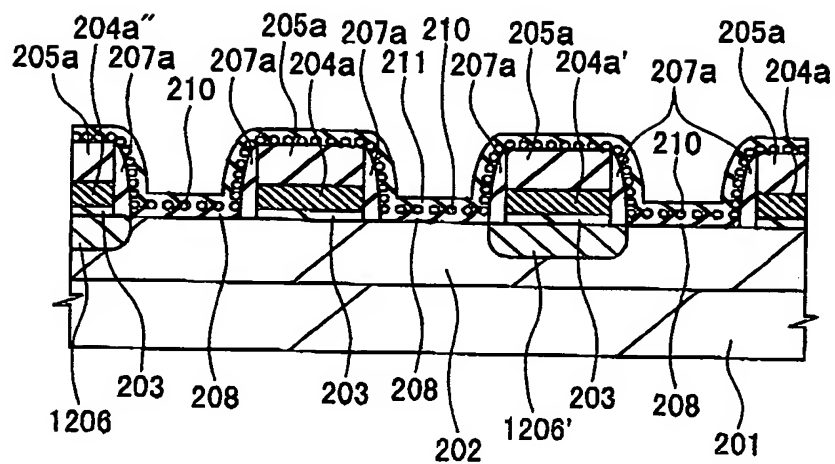


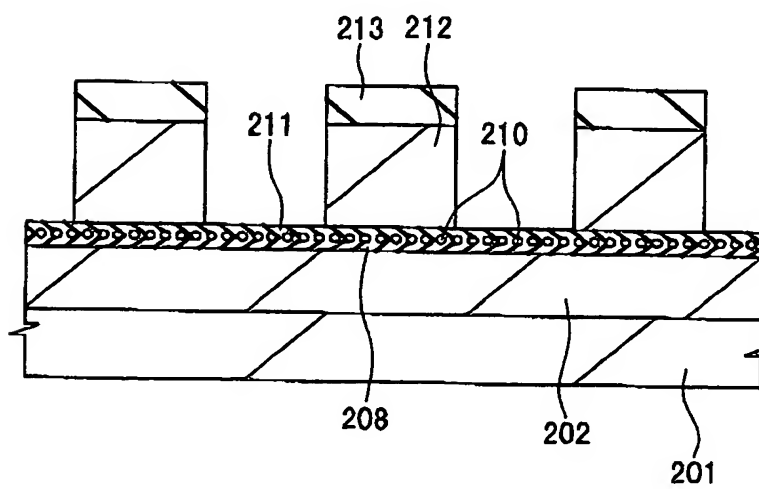
FIG.55



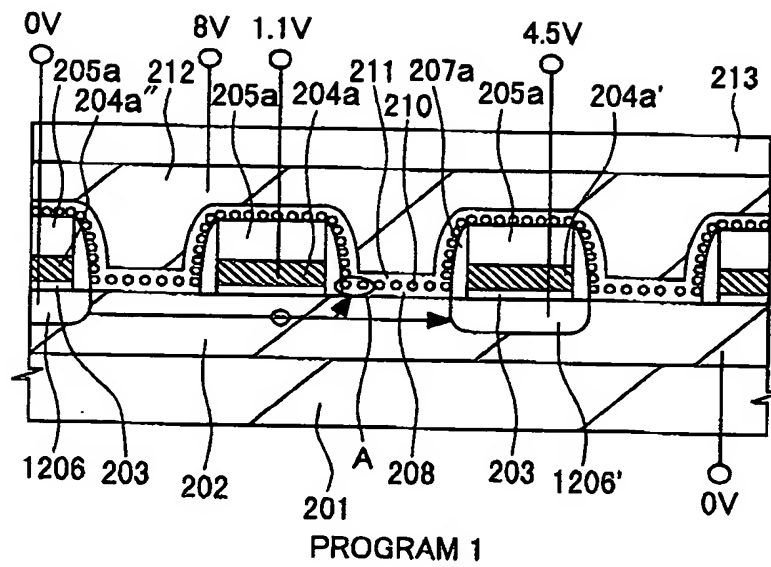
**FIG.56**



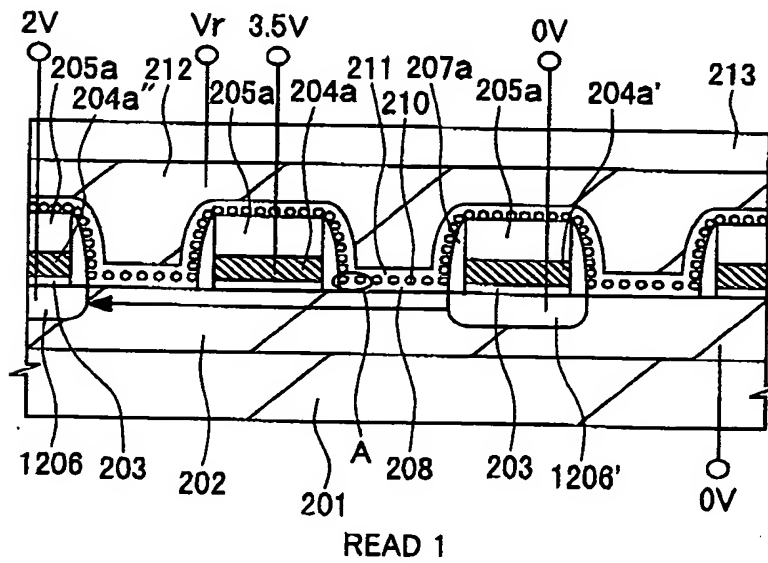
**FIG.57**



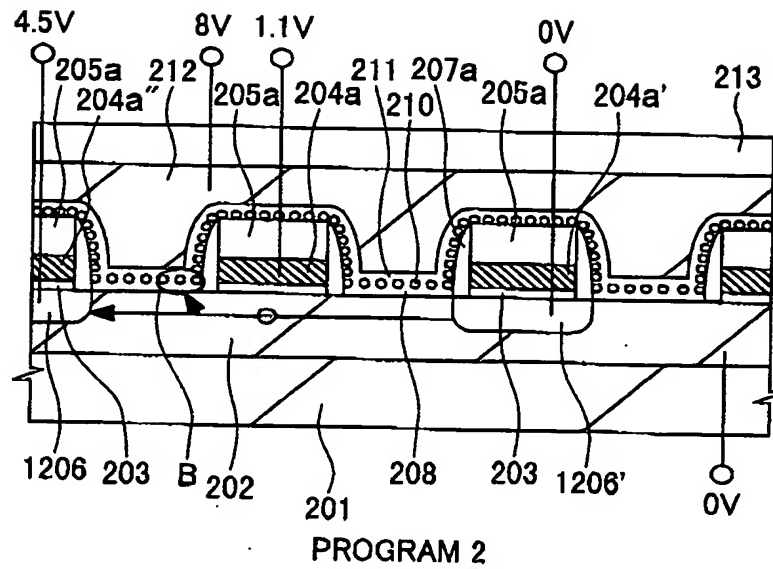
# FIG.58



# FIG.59



# FIG.60



# FIG.61

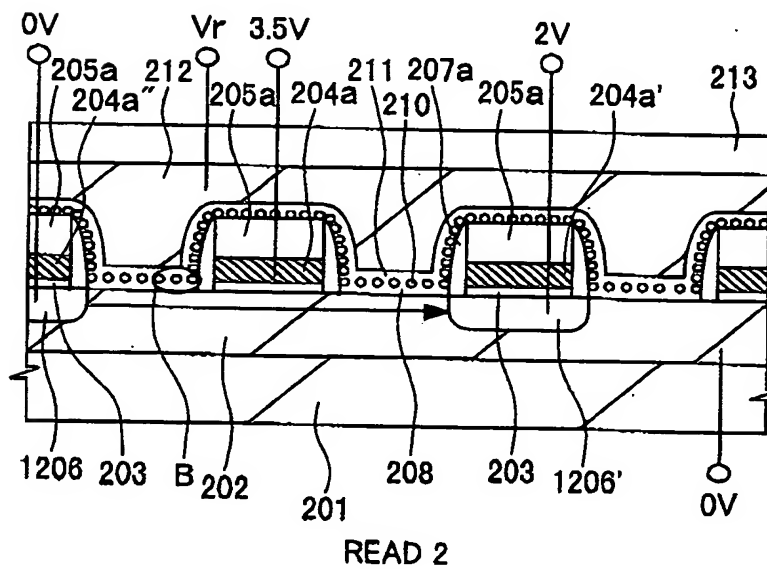




FIG.62

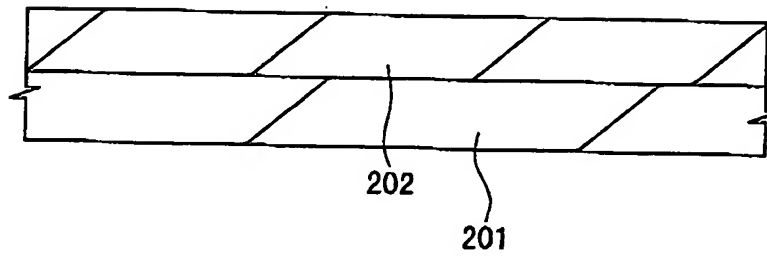


FIG.63

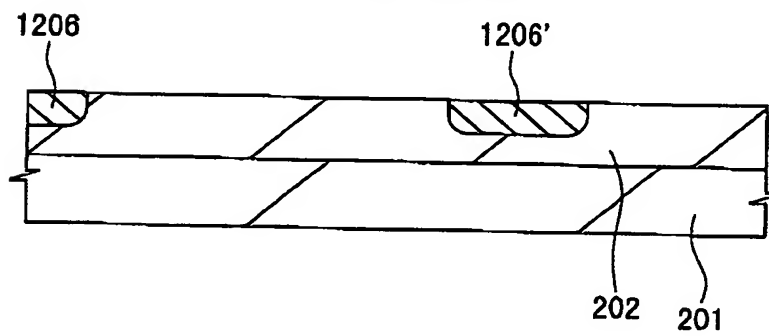
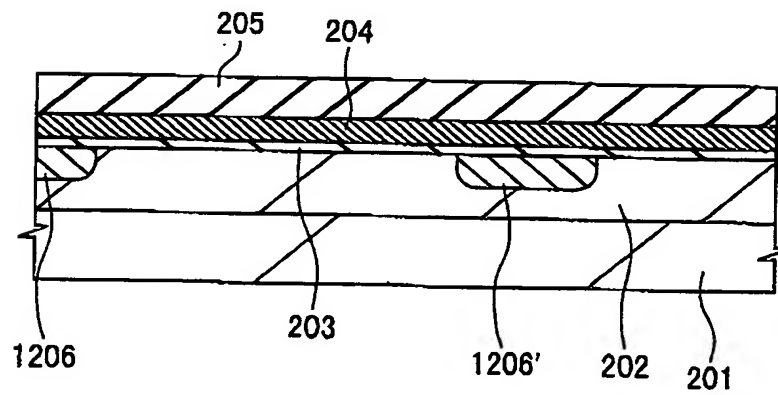
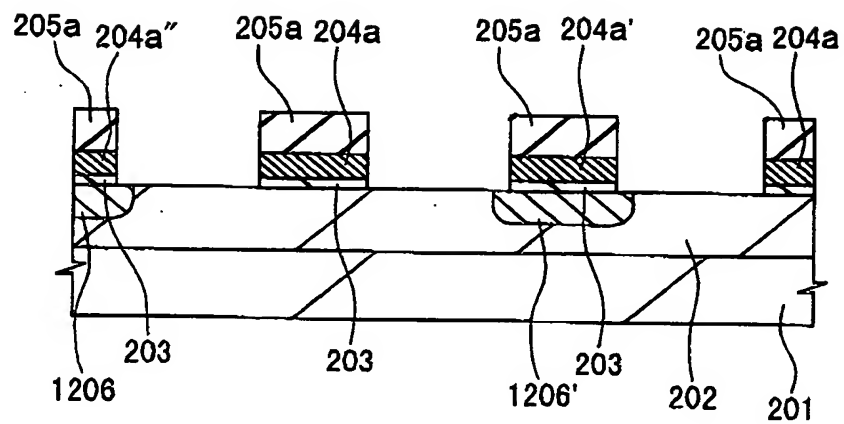


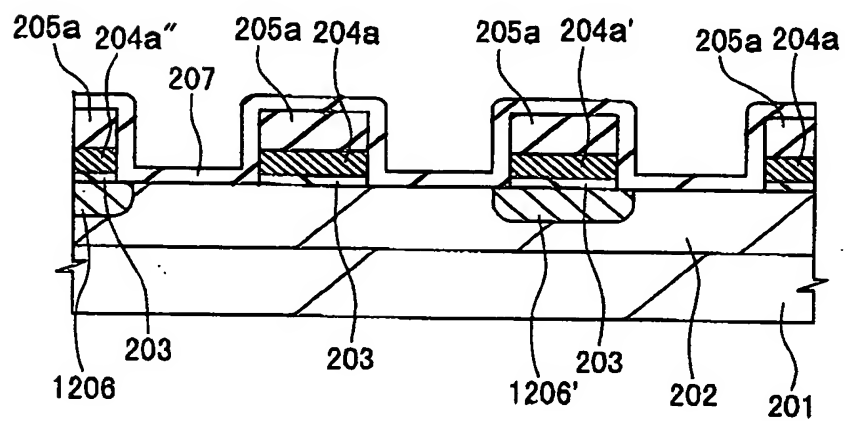
FIG.64



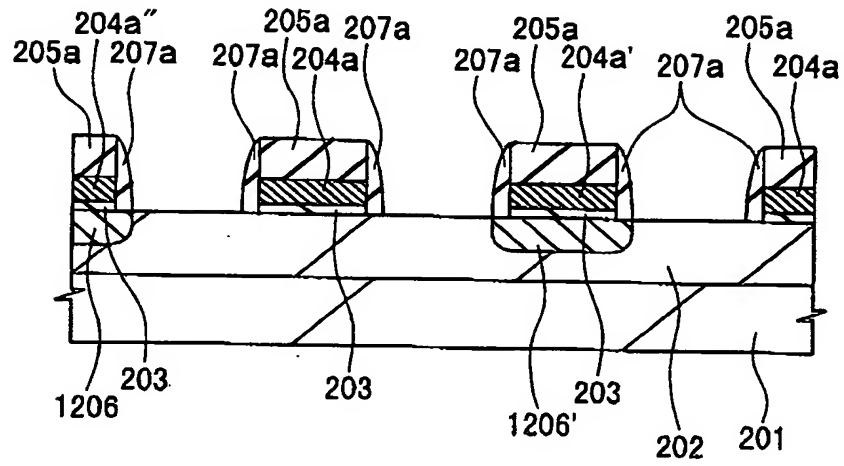
# FIG.65



# FIG.66



# FIG.67



# FIG.68

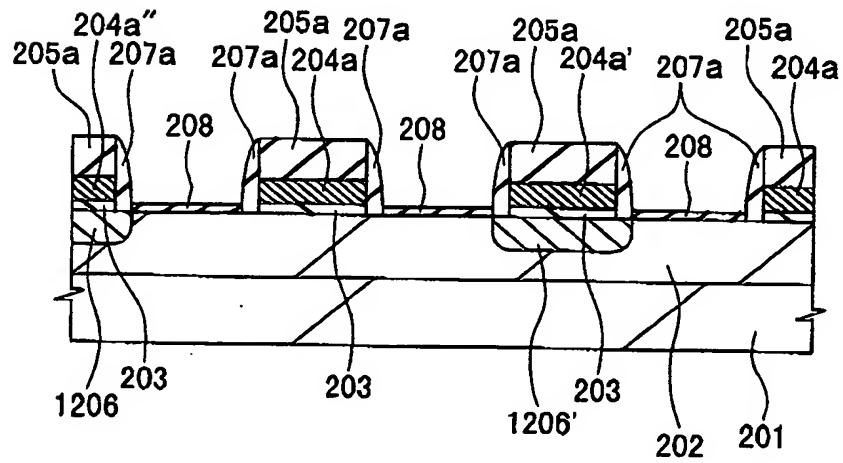
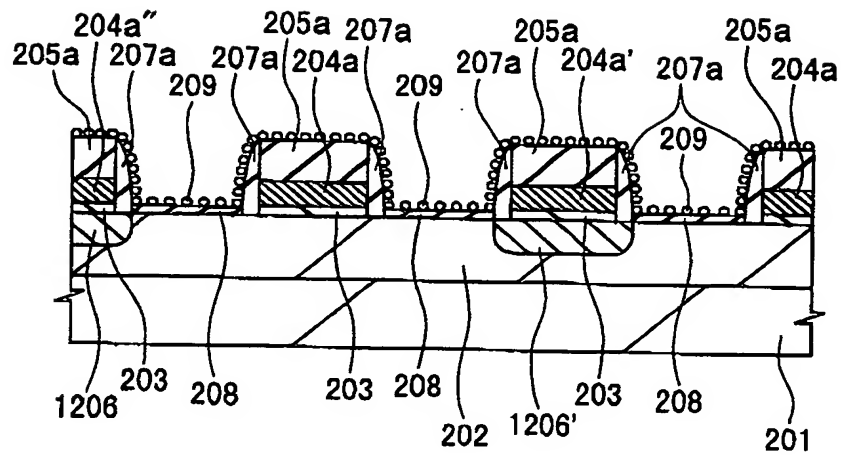
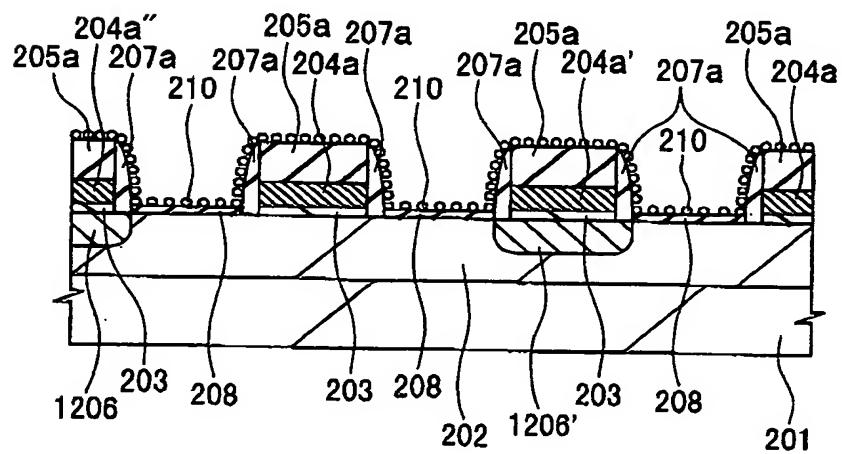


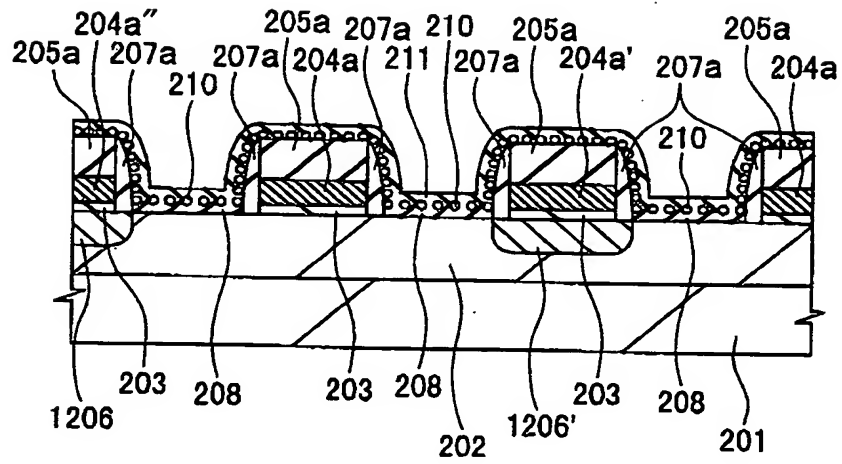
FIG. 69



**FIG.70**



# FIG.71



# FIG.72

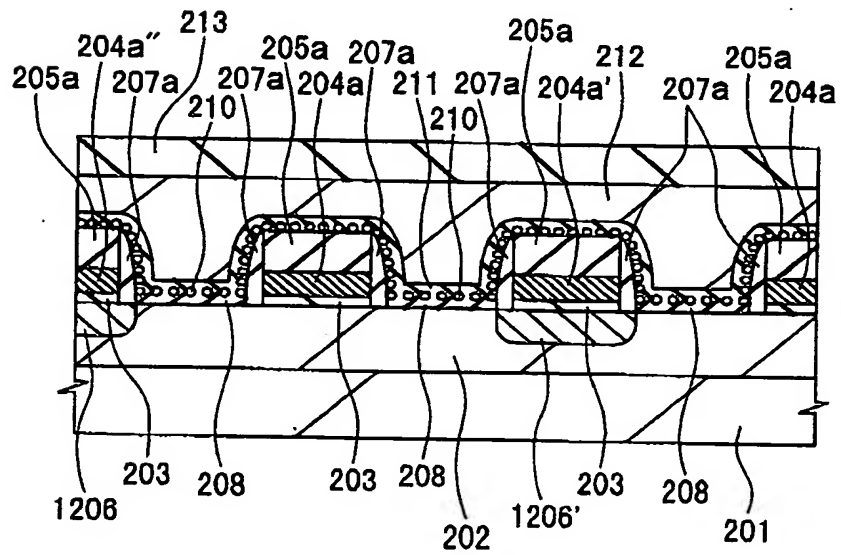


FIG.73

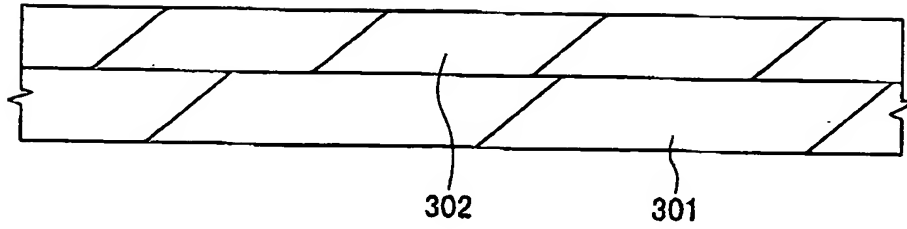


FIG.74

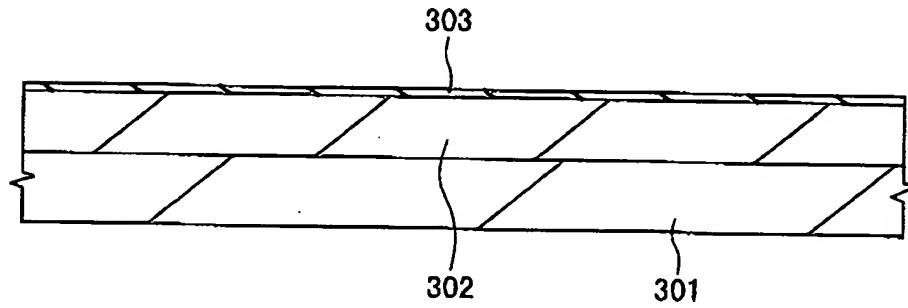


FIG.75

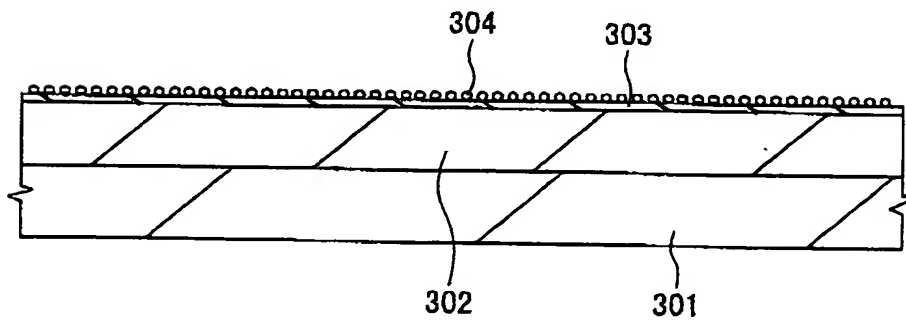


FIG.76

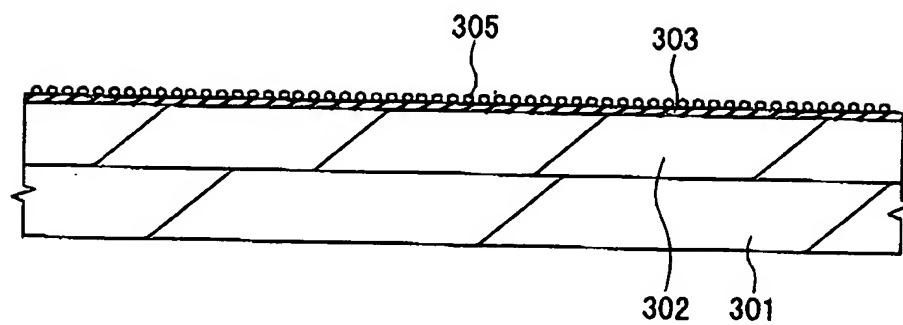
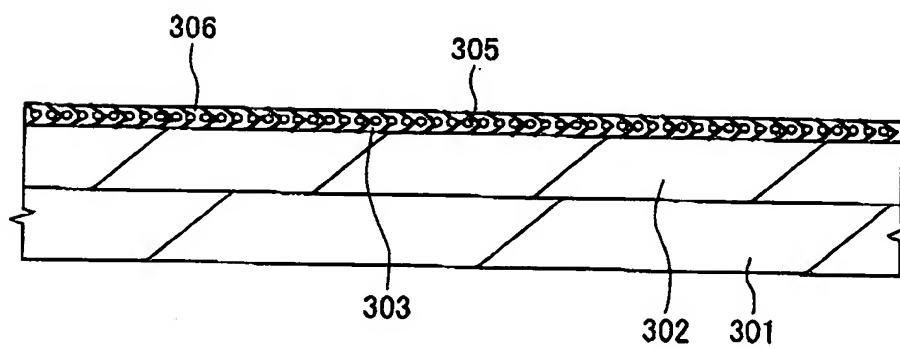
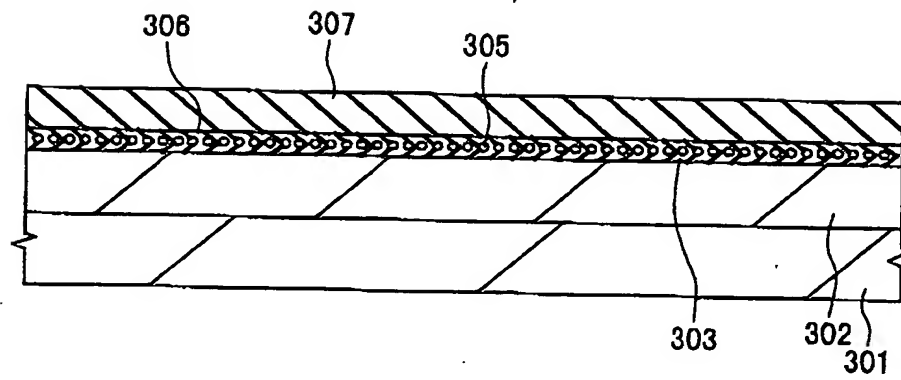


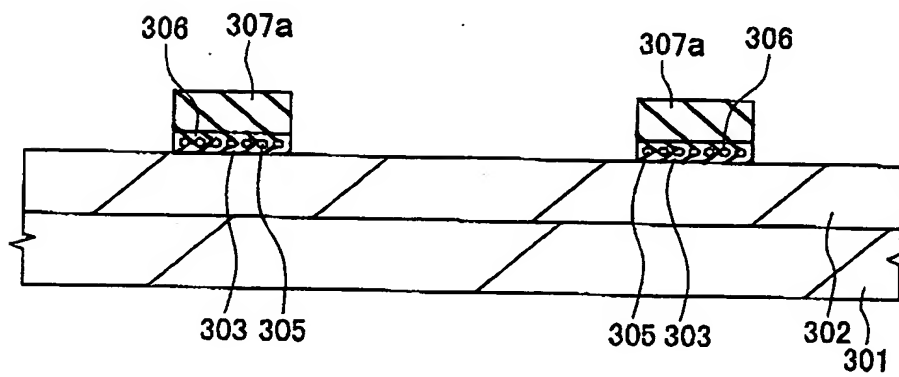
FIG.77



# FIG.78

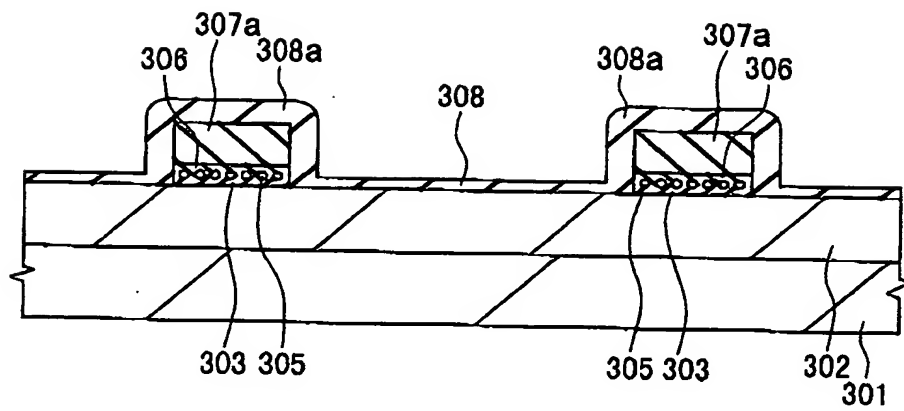


# FIG.79

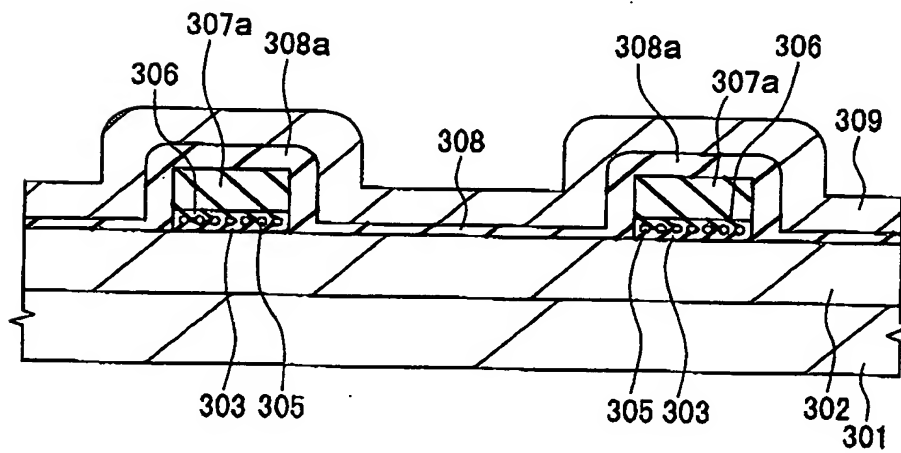




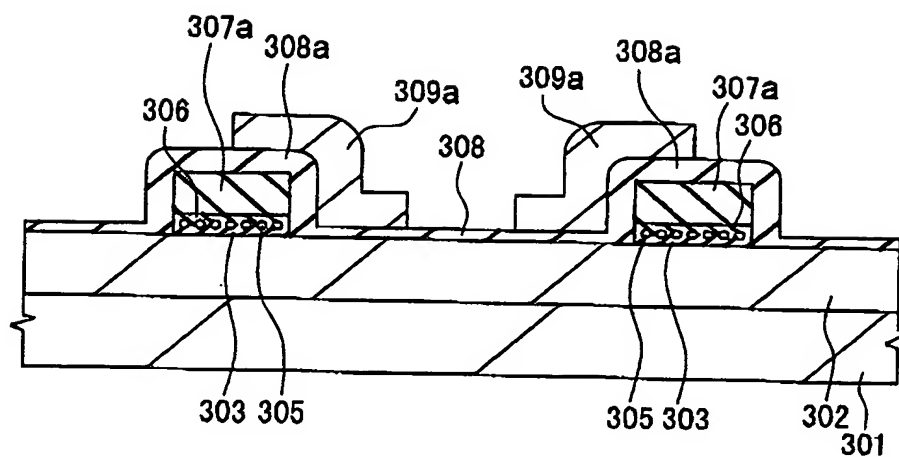
# FIG.80



# FIG.81



# FIG.82



# FIG.83

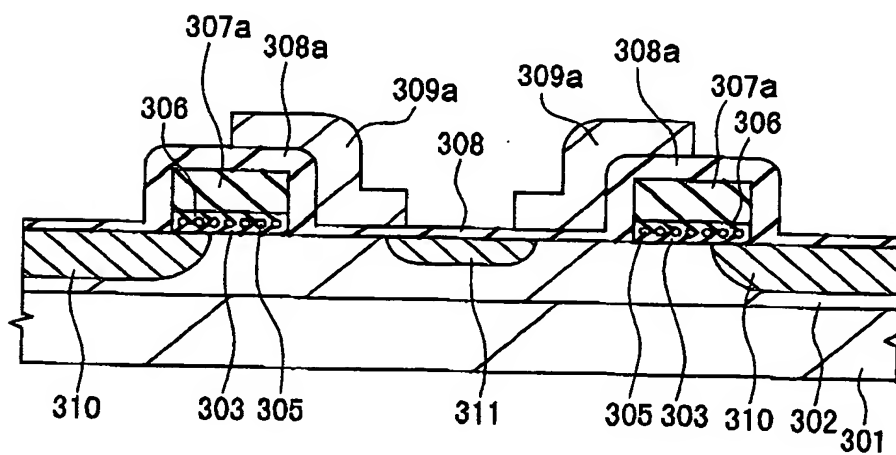


FIG.84

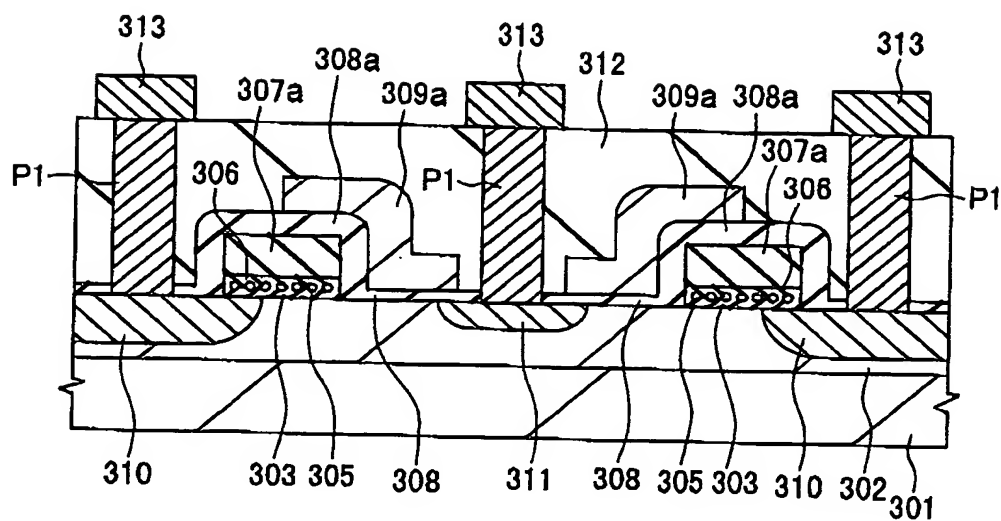
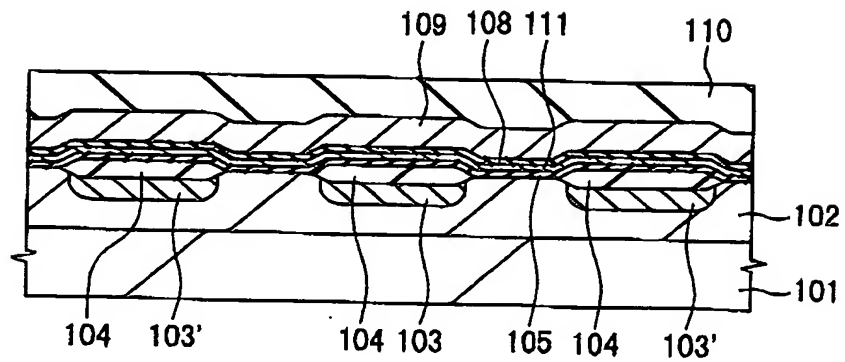
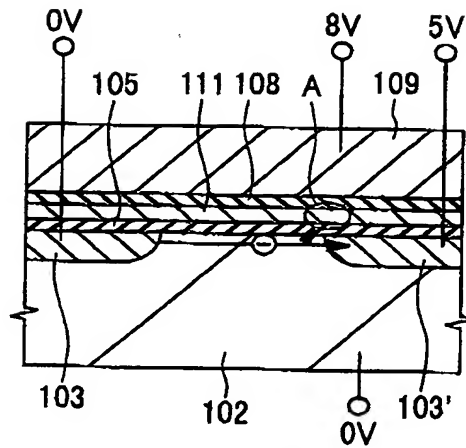


FIG.85

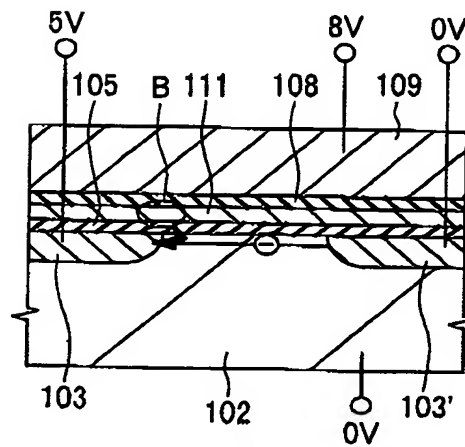


# FIG.86



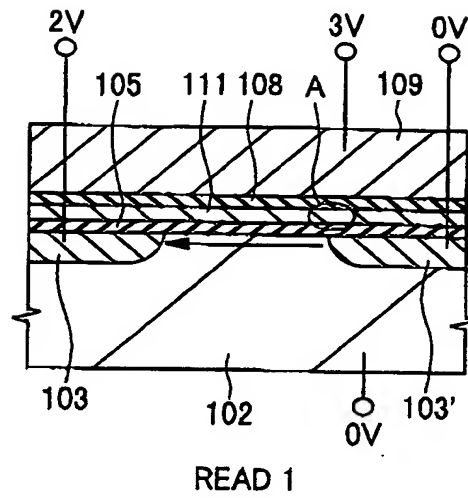
PROGRAM 1

# FIG.87



PROGRAM 2

# FIG.88



# FIG.89

